Improving SMT Yield and Reducing Defects: A Rauland Case Study

Article by Edward Hughes
ACULON

Ever-increasing demand for more complex boards that have higher densities of components means more challenges for SMT assembly operations and yields. Smaller component sizes and more densely packed PCBs lead to more powerful designs in much smaller product packages. These advancements have spurred a new set of challenges in building smaller and more complex assemblies.

Even though SMT products have been manufactured in high volume for decades, SMT line issues continue to be prevalent and new demands continue to pose new challenges. While the SMT print process is not complicated, controlling the outcome is complex. Having an underperforming SMT process results in lots of rework, lower throughput and added product costs as well as product reliability issues.

Rauland, a division of AMETEK Inc., is an 80-year integrated communications technology company that builds nurses call stations and school bell systems. The company responds to market needs globally with two distinct communication system product lines: Responder, designed for the healthcare industry; and Telecenter systems, which serve the educational market.

SMTA-certified Process Engineer Jimmy Crow works at Rauland's highly sophisticated, FDA-compliant manufacturing facility that has state-of-the-art SMT equipment. At Rauland they build four- to eight-layer PCBs, place BGA, PCBGA, QFNs, typical double-sided boards, with its smallest part to date an 042 Aperio.

Disciplined and quality conscious, Crow was not happy with the performance of his SMT line. There were too many defect and too much line downtime. Rework levels were also too high. His goal was to reduce SMT related defects and increase throughput while maintaining quality.

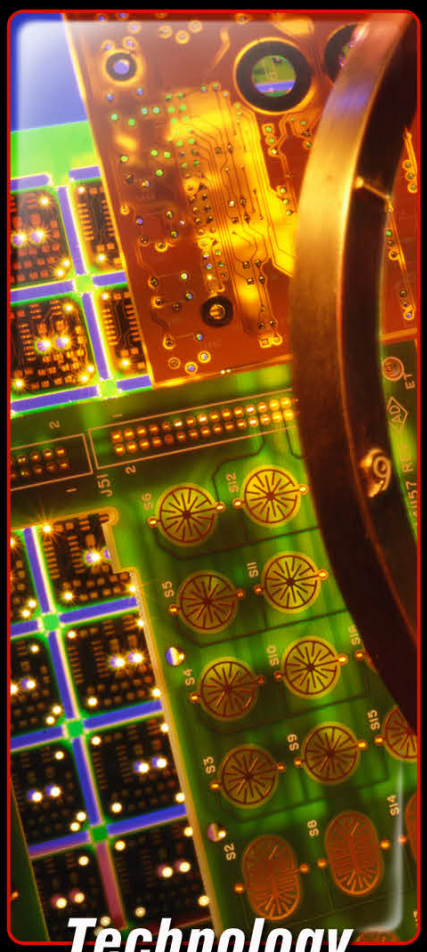
Studies have shown that 65% of defects from SMT lines comes from the screen-print-

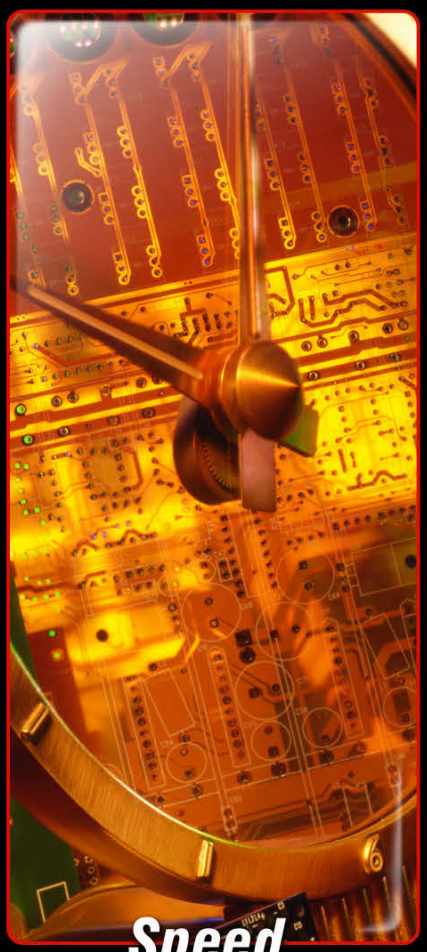
APEX EXPO IPC 2018 Booth #916

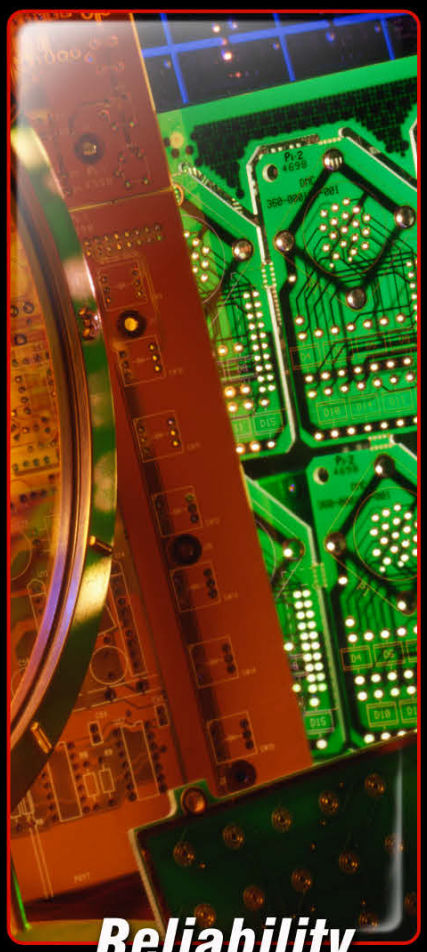
prototron.com

We Take the Time to do it Right

because you don't have the time to do it over.







Prototron Circuits

High quality quick turn manufacturing, just another reason we are

America's Board Shop

Redmond Facility
15225 NE 95th Street, Redmond, WA 98052
Toll: 888.847.7686 Phone: 425.823.7000

Tucson Facility
3760 E. 43rd Place, Tucson, AZ 85713
Toll: 800.279.5572 Phone: 520.745.8515

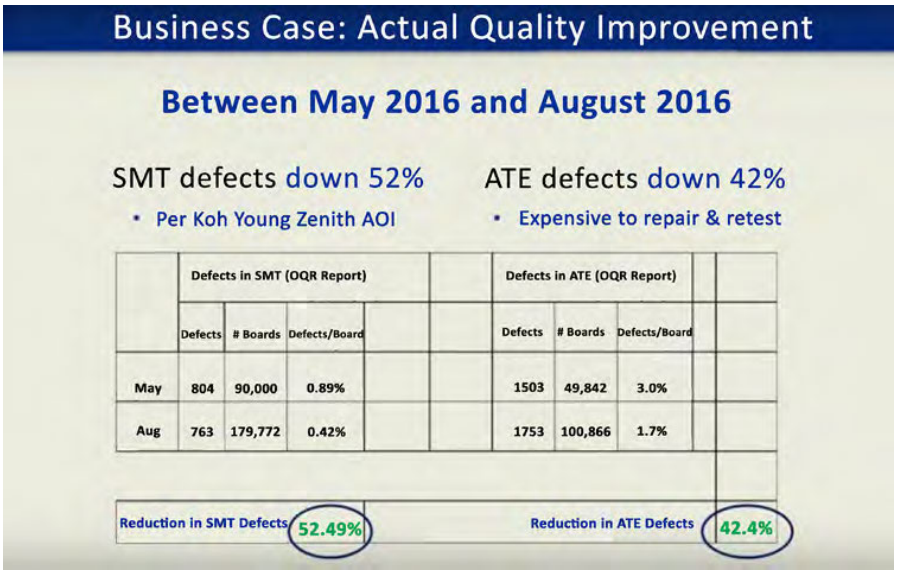


Figure 1: Jimmy Crow delivered terrific results for Rauland: SMT-related defects were reduced by over 50%; throughput was increased by over 20%, and the company saved $1 million per year for three SMT lines.

ing process, and Crow felt this was certainly the case in his factory. With a 22-second mean cycle time, the stencil printer was the gating process on the assembly line because it was stopped every two and a half minutes for cleaning. As a result, the SMT line would be empty of boards. The line badly needed balancing as no one wants the stencil printer to be the slowest item on assembly line.

To achieve this, Crow started by concentrating on the screen printing process, which has the largest impact over yield, throughput, quality, and downtime costs. He concentrated primarily on process improvements. Crow began a systematic root cause analysis of the defects.

1. Under Screen Cleaning

Crow's initial focus was on the substances that clean the screen mechanically—the "paper" and the under-screen solvents used. After investigating different types of paper, Crow found there were better options out there than the current product. He selected a more porous wipe material that he thought would allow for better wiping. The Micro-Care Stencil easily handled the sharp edges on the SMT stencil, which often shredded old-style stencil wipes, causing defects and rework. The structure of the open paper also captures solder balls better than some of the closed structure fill papers.

2. Solvents

Crow then turned his attention to under-screen solvents. IPA (isopropyl alcohol) was problematic because newer solder pastes are comprised of synthetic resins, and the alcohol made the solder viscosity and machinery difficult to maintain. The cleaning properties were not good enough with IPA, as it did not clean and caused some paste bricks to cling to the aperture walls. He even turned off the IPA and sprayed nothing, and experienced the same results. So, he knew he needed to find a better solvent.

For the solvent, he wanted something that was efficient without being harmful to the screen printer. He ultimately chose Zestron Vigon UC160, an aqueous-based cleaning medium specifically designed for SMT stencil. The water based formulation evaporates more slowly than IPA, but could clean with less wipes.

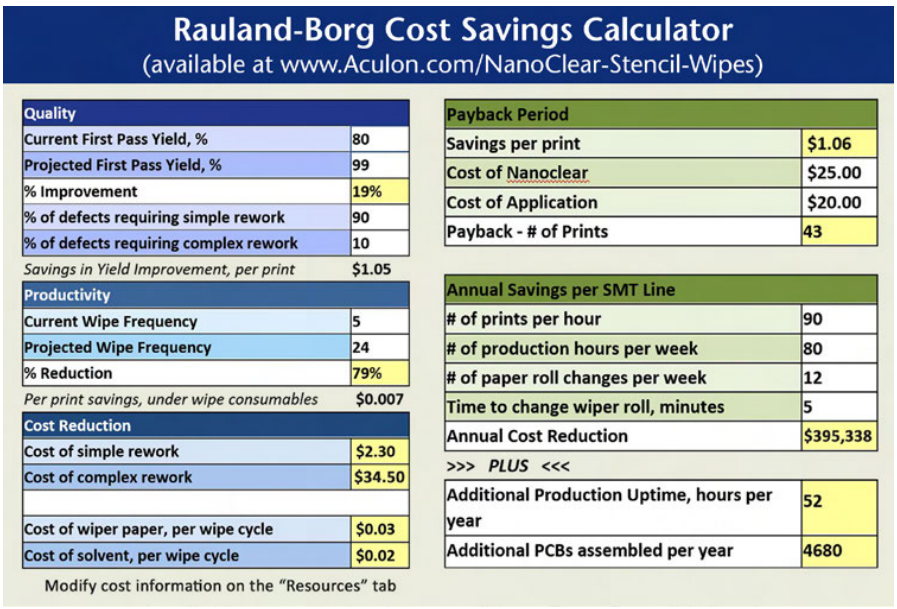
3. Nanocoating

In taking a systemic view of his SMT line issue, Crow had found a better paper and a better solvent, but he was still experiencing defects and downtime. They were still wiping every four to five boards based on the complexity of the stencil. Something was missing to make the process improvement complete.

That was when Crow met an SMT manufacturing expert, Chrys Shea, at an industry conference and found she had been conducting the same SMT line improvement programs and had delivered remarkable results. Her scientific approach to solving the SMT line

issues mirrored Crow's, but she had already found the missing ingredient that he was looking for, a nanocoating. Shea's research had led her to advocate Aculon's NanoClear, a stencil treatment technology, for several years as she had been able to demonstrate significant improvements in performance across many SMT lines.

When Crow added NanoClear to his SMT process, he followed Shea's advice and expected to double under-stencil wipe cleaning every fourth or fifth board to every eighth or ninth or tenth board. With Aculon's NanoClear, Crow's throughput was increased by a third and the factory's defect as tracked by Koh Young Zenith and AOI dropped by 52%. All his projections were blown away. Crow's line could now run 24 print cycles before cleaning. Their AOI and ATE tests saw no reduction in quality. With a faster screen printer, a faster SMT line and a cleaner process, Crow maintained improved quality while running faster.



Rauland-Borg Cost Savings Calculator
(available at www.Aculon.com/NanoClear-Stencil-Wipes)

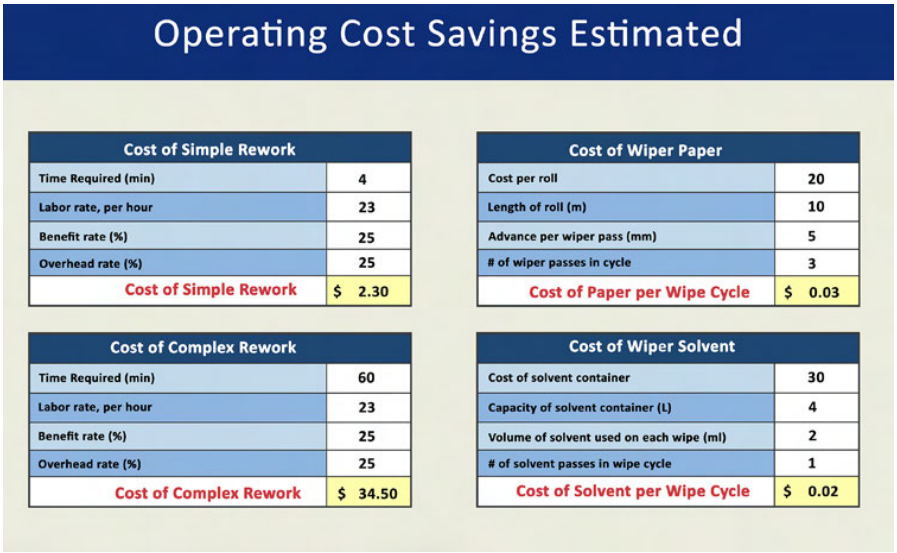
Quality	
Current First Pass Yield, %	80
Projected First Pass Yield, %	99
% Improvement	19%
% of defects requiring simple rework	90
% of defects requiring complex rework	10
Savings in Yield Improvement, per print	$1.05
Productivity	
Current Wipe Frequency	5
Projected Wipe Frequency	24
% Reduction	79%
Per print savings, under wipe consumables	$0.007
Cost Reduction	
Cost of simple rework	$2.30
Cost of complex rework	$34.50
Cost of wiper paper, per wipe cycle	$0.03
Cost of solvent, per wipe cycle	$0.02

Modify cost information on the "Resources" tab

Payback Period	
Savings per print	$1.06
Cost of Nanoclear	$25.00
Cost of Application	$20.00
Payback - # of Prints	43

Annual Savings per SMT Line	
# of prints per hour	90
# of production hours per week	80
# of paper roll changes per week	12
Time to change wiper roll, minutes	5
Annual Cost Reduction	$395,338
>>> *PLUS* <<<	
Additional Production Uptime, hours per year	52
Additional PCBs assembled per year	4680

Figure 2: With the cost calculator, management could easily see the result of the process improvement program.



Operating Cost Savings Estimated

Cost of Simple Rework	
Time Required (min)	4
Labor rate, per hour	23
Benefit rate (%)	25
Overhead rate (%)	25
Cost of Simple Rework	$ 2.30

Cost of Wiper Paper	
Cost per roll	20
Length of roll (m)	10
Advance per wiper pass (mm)	5
# of wiper passes in cycle	3
Cost of Paper per Wipe Cycle	$ 0.03

Cost of Complex Rework	
Time Required (min)	60
Labor rate, per hour	23
Benefit rate (%)	25
Overhead rate (%)	25
Cost of Complex Rework	$ 34.50

Cost of Wiper Solvent	
Cost of solvent container	30
Capacity of solvent container (L)	4
Volume of solvent used on each wipe (ml)	2
# of solvent passes in wipe cycle	1
Cost of Solvent per Wipe Cycle	$ 0.02

Figure 3: The cost calculator considers the costs of rework, both simple and complex, the cost of wiper paper, and the cost of the solvent.

The Numbers

Crow thought he had found the trifecta—softer wiper paper, engineered solvents and a nanocoating. As a result, Crow delivered terrific results for Rauland: SMT-related defects were reduced by over 50%; throughput was increased by over 20%, and the company saved $1 million per year for three SMT lines. First pass yield went from 80% to 99%. The line had a 79% reduction in under-stencil wiping as the interval went from five prints per wipe to 24 prints per wipe.

Using the downloadable cost of ownership calculator Shea created for Aculon, Crow could

demonstrate to management the result of his process improvement program. In calculating savings, the cost calculator considers the costs of rework, both simple and complex, the cost of wiper paper, and the cost of the solvent. Using the calculator, Crow could determine that the cost per board for simple rework was $2.30 per board compared with $34.50 per board for the cost of complex rework. In addition, the cost of paper was just $0.03 per board and the cost of solvent was $0.02 per board.

By combining the rework savings along with the reduction in paper and solvent used due to less under-stencil wiping, the annual savings demonstrated from using the calculator were considerable. In addition, as Crow's team was not changing wiper rolls as often, he was getting an extra 52 hours—over a full shift week—of additional production a year. For his investment, Crow produced an additional 5,000 boards a year. With approximately 200 stencils at a cost of $25 an application, a total investment across all stencils is about $5,000—to save $395,000.

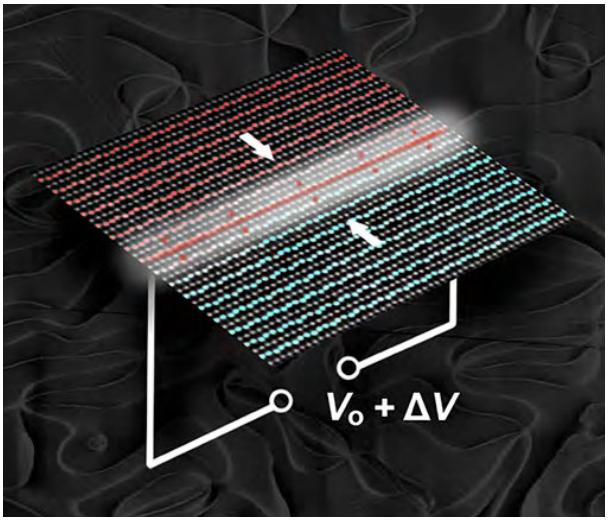
Crow's management recognized the magnificent work by giving him a bonus and promotion. So, what can we say, but, 'Well done Jimmy!' Here's to a job well done. **SMT007**

Edward Hughes is the chairman and CEO Aculon.

Rewritable Wires Could Mean No More Obsolete Circuitry

Ferroelectric materials have spontaneous electrical ordering that can be changed by applying an electric field. Where two domains of different polarizations meet, it is called a ferroelectric domain wall. These domain walls are promising for next-generation circuit elements due to their unusual electronic properties and because they can be formed, moved, and erased on demand.

Scientists envision a transistor where the gate is a domain wall itself–and whether you can pass current through the domain wall is controlled by the charges in the domain wall. Now, scientists have found that they can reversibly switch domain walls between being resistive or conductive depending on the electric field they apply.



Using atomic-resolution electron microscopy and spectroscopy, they found that the electrons that move to the wall were confined to just one to two repeating crystalline unit cells in erbium manganite ($ErMnO^3$). When the polarizations of the two ferroelectric domains point at each other (head-to-head), there is nominally a buildup of positive charge at the domain wall. This positive charge was compensated by extra electrons that accumulated on the atoms within the domain wall. These electrons were stuck, shielding the local charges, and did not conduct.

By applying an electric field, extra electrons flowed into the channel at the domain wall. When all the local charges were sufficiently shielded, the electrons in the channel were free to move within the domain wall, forming a 2-D conductive sheet. This conductive sheet could be used as a switch or transistor. The switch is "off" when current does not flow. Applying an electric field allows current to pass, turning the switch "on." This paves the way towards developing all-domain-wall electrical devices.